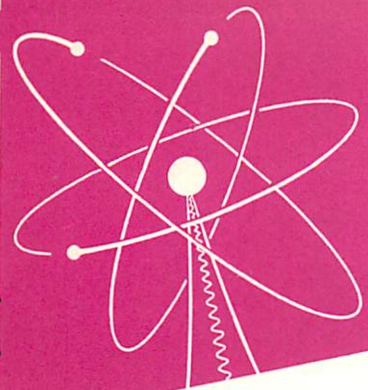

CAMERA CONTROL UNITS

Lesson T4E-4A

DeVRY Technical Institute
4141 W. Belmont Ave., Chicago 41, Illinois
Formerly DeFOREST'S TRAINING, INC.

T4E-4A

CAMERA CONTROL UNITS

DeVRY Technical Institute
4141 Belmont Ave.
Chicago 41, Illinois

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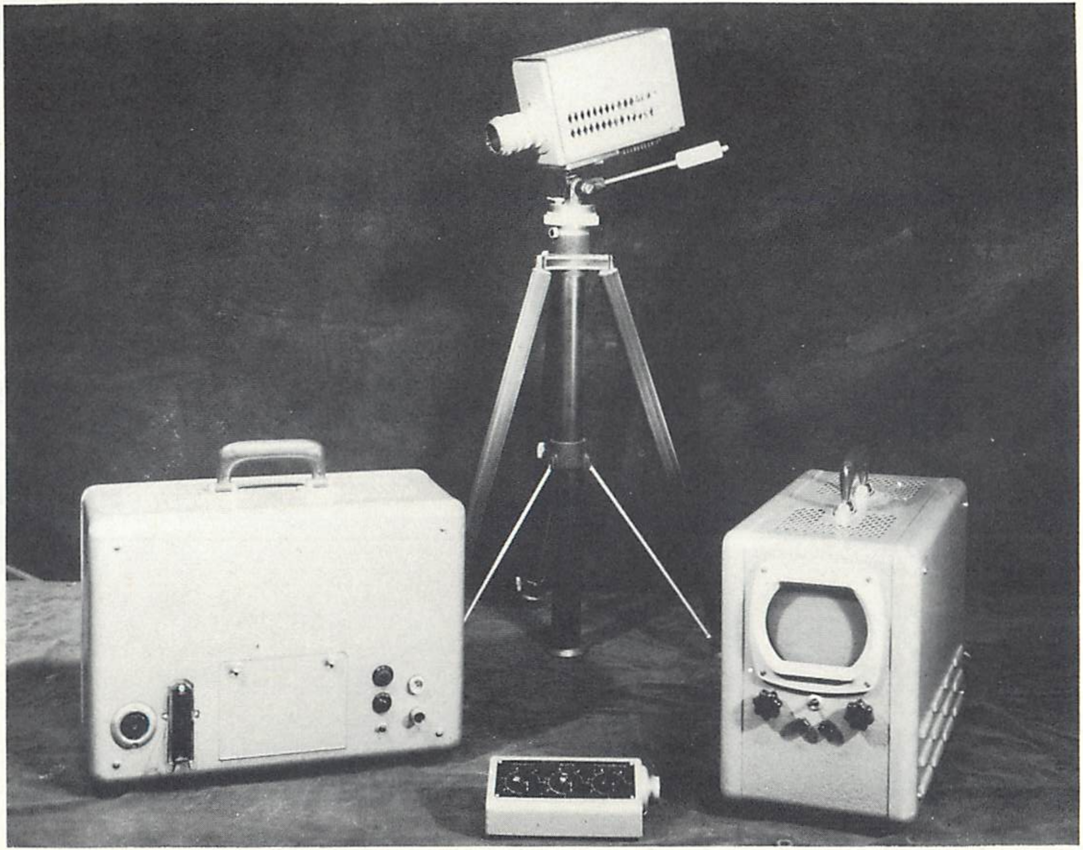


A complete industrial closed circuit TV system consisting of camera, tripod, remote control box, and camera control unit. Its compactness renders it completely portable.

Courtesy Curtiss-Wright Corporation

CAMERA CONTROL UNITS

Contents

PAGE

Timers and Sync Generators 6
  Oscillators 6
  Dividers 7
  AFC Discriminator 9
  Complete Timer 13
Blanking Generator 16
Complete Camera Control 17
  Power Supply 18
  Timer 18
  Vertical Deflection 22
  Horizontal Deflection and High Voltage 22
  Blanking and Sync Generation 23
  Video Amplifier Circuits 24
  The R-F Unit 26

> **No field of endeavor ever proposed by man offers more or demands more from its patrons than does the creation and transmission of electronic pictures. If people engaged in television work disregard the idea of associated professions, they might nullify possible contributions to the art. No one person can feel that his knowledge of a specialty is in itself sufficient or that knowledge of the potentialities and problems of his colleagues are not required. Television is, in truth, a melting pot of the sciences, the arts, and the populace.**
>
> **—Selected.**

CAMERA CONTROL UNITS

Many of the complete camera chains that are used in present day closed circuit TV systems do not provide a standard 525 line, interlaced picture. As mentioned in the preceding lesson, this non-use of interlace is permissible because the signal is not communicated by means of electromagnetic radiations. The FCC rules and regulations that govern conventional TV systems do not apply to closed circuit TV and allow the designers of the equipment greater freedom to carry out their ideas.

As a consequence, some cameras contain only those components that are absolutely necessary such as the vidicon camera tube, its associated components, a video preamplifier and the interconnecting cable to the camera control unit.

Other cameras are very elaborate and contain the complete deflection system for the vidicon, a multiple stage video amplifier, sync pulse amplifiers, blanking pulse amplifiers, r-f oscillator and modulators, automatic target control circuits and vidicon protection circuits. In fact, some cameras contain the timer units that produce the pulses used to synchronize the deflection circuits of the monitor with those of the camera. These cameras are essentially self contained units and require only a monitor or a TV receiver to complete the entire chain.

This great flexibility of equipment is very advantageous to both the manufacturer and the purchaser of the equipment. It enables the purchaser to obtain equipment that will best suit his needs at the lowest possible price. For example, if the equipment is to be used to observe large objects on an assembly line, the frequency response would not have to be on a par with a conventional television receiver and it would not be necessary to have interlaced scanning or wide-band video amplifiers.

This same situation is also advantageous to the manufacturer as it enables him to sell equipment to industries which might not be able to afford the expense of a more elaborate closed TV system.

On the other hand, there are some instances where conventional TV systems are not adequate to meet the requirements that would be demanded of it. The TV system that enables internes and other interested medical personnel to observe highly skilled surgeons perform actual operations would require a very high quality picture. A system employing more than 525 lines and capable of reproducing a picture that contains fine detail up to 5 or 6 megacycles is often used. In fact, these systems are sometimes designed to reproduce a complete color picture to increase its value still more.

This flexibility of equipment, with all of its advantages, can present a problem to the electronic technician who has the responsibility of maintaining it. The technician who services television receivers has his work simplified considerably by the fact that all TV receivers are basically the same. He knows that the receiver contains a tuner, a video i-f strip, a video detector, a video amplifier, a sound section, vertical and horizontal deflection circuits, sync circuits, and the high voltage circuits. Even though the variations in these circuits are numerous, each one must be present and must do a particular job.

As you progress through these closed circuit TV lessons, it will become increasingly evident that these similarities of construction are not maintained by the manufacturer of industrial TV equipment. Accordingly, it is impossible to say that certain functions of the complete camera chain will be performed by a particular part of the camera chain. One manufacturer, for example, mixes the sync and blanking pulses with the video information in the camera and feeds this composite signal to the monitor. Another manufacturer mixes the sync and blanking pulses with the video in the camera control, while still a third manufacturer does not mix the sync pulses with the video but feeds the vertical and horizontal sync pulses on separate coaxial cables to the camera deflection circuits and to the monitor deflection circuits.

The operation of an important piece of factory machinery is being carefully observed in an overhead office.

Courtesy Allen B. DuMont Laboratories, Inc.

In these closed circuit TV lessons, an attempt is made to divide the equipment into three main classifications; namely, (1) the camera, (2) the camera control, and (3) the monitor. The various equipment described is some of the equipment that is now being used. It was chosen to cover a wide variety and to give the student a good idea of what is to be expected in the commercial field.

TIMERS AND SYNC GENERATORS

A good percentage of the present day closed circuit TV equipment provides a standard 525 line, interlaced picture. In order to accomplish this standard, the sync pulses that control the horizontal and vertical deflection circuits of the camera and the monitor must be derived from a single master oscillator the frequency of which is 31.5 kc. The output of this oscillator is then fed into a circuit which produces one output pulse for every two input pulses providing a signal of 15,750 cps. The circuit used to perform this division by two is called a **divider.**

The output of the 31.5 kc master oscillator is also fed into a series of divider circuits which provide a division by 525 to obtain a 60 cps pulse that is synchronized with the 15,570 cps pulse.

Oscillators

The circuit that is used as the master oscillator can be a tuned circuit in which the frequency is determined by the values of inductance and capacitance in the resonant circuit. The master oscillator also can be a blocking oscillator, a multivibrator or any other oscillator that the designer sees fit to use.

In Figure 1, the master oscillator is a blocking oscillator type consisting of V_1 and its associated components. The 31.5 kc pulse is fed through C_2 to the grid of V_2 which is another blocking oscillator. The free-running frequency of V_2 is approximately 4.5 kc and is controlled by adjusting R_4. Since the master oscillator frequency is 31.5 kc and the V_2 oscillator frequency is only 4.5 kc, the V_2 circuitry is identified as a divider. In this particular case, the divider operates at one-seventh of the master oscillator frequency and is functioning as a "÷7" divider.

In order to get a better understanding of the manner in which the divider circuits function, let us examine the blocking oscillator circuit of Figure 2. The free-running frequency is determined by the values of C_2, R_2 and R_3 with R_3 being variable so that the frequency of oscillation can be adjusted to a certain extent.

When the tube first starts to conduct, the electron path is from cathode to plate of V_1, through the primary winding of T_1 to B+. This conduction causes the plate side of the T_1 primary to become less positive and induces a voltage into the secondary which, due to the reversal of phase in the transformer, causes the voltage applied to the grid of V_2 to become more positive. A more positive voltage on the grid causes the plate current to increase still more and the action of the transformer causes the grid voltage to become more positive.

This action very quickly causes a condition of plate current saturation and, because the grid is driven positive in respect to the cathode, the grid draws current which charges C_2 negative on its right hand plate and positive on its left hand plate. This charge on C_2 biases V_1 to cutoff and plate current ceases. With C_2 no longer charging, it immediately begins to discharge. Electrons leave the right hand plate, pass down through R_2 and R_3 to ground. From ground they travel up through R_1 and through the secondary winding of T_1 to the left hand plate of C_2.

As C_2 discharges, the voltage developed across R_2 and R_3 becomes less negative. When C_2 has discharged to a point where the voltage across R_2 and R_3 is not sufficient to hold V_1 at cutoff, the tube begins to conduct and the entire cycle repeats.

Figure 3A is the wave-form that is developed between the grid of V_1 and ground. The portion of the wave-form above the zero axis represents the period of time when the feedback due to T_1 drives the grid positive and causes grid current. The rapid negative swing immediately following the positive pulse is caused by the charge on C_2. The gradual reduction of the negative voltage represents the discharge of C_2 and this continues until the tube comes out of cutoff and the grid is once again driven positive.

This unit is completely self contained even to the point of having a built-in view finder. A monitor is the only other piece of equipment necessary to form the complete camera chain.

Courtesy Dage Television Division—
Thompson Products, Inc.

Dividers

This blocking oscillator can be synchronized quite readily by adjusting R_3 so that its free-running frequency is slightly lower than the frequency of the positive pulses used for synchronization. The pulses cause the tube to come out of cutoff slightly before it normally would and force it to oscillate at the frequency of the sync pulses.

It is also possible to design the oscillator so that it is triggered by every second sync pulse rather than by every sync pulse. Figure 3B shows the wave-form that is present under these conditions. Notice that the positive pulse occurs at about the middle of the slope portion of the wave-form and is not of sufficient amplitude to bring the tube out of cutoff. These pulses do not have any effect upon the oscillator and thus the oscillator is synchronized by every second pulse. This means that plate current pulses will be exactly one-half the frequency of the incoming sync pulses.

This "divider" action can be carried even further and the blocking oscillator components can be chosen so that almost any division is obtained. Figure 3C shows the wave-form that is present on the grid of V_1 in Figure 2 when the circuit is designed to function as a "÷5" divider. Here, four of the incoming sync pulses have no effect and the oscillator is triggered by the fifth pulse. This fifth pulse is not seen as it is covered by the pulse action of the oscillator which drives the grid positive.

Going back to the circuit of Figure 1, the 31.5 kc pulses from V_1 are coupled through C_2 to the grid of V_2. R_4 is used to adjust the frequency of V_2 so that every seventh pulse triggers V_2 into conduction. These plate current pulses of V_2, which are at a frequency of 4.5 kc, are coupled through R_7 to the next divider to accomplish further division.

Point "B" at the junction of C_4 and R_6, provides a scope test point. C_4 is a small capacitor and provides isolation between the scope and the blocking oscillator grid circuit. This network prevents the input impedance of the scope from affecting the grid circuit of V_2 and permits adjustments to be made while the circuit is in operation.

Another point of interest in this circuit is that the controls in the grid circuits of the two blocking oscillators are returned through R_5 to B+ rather than to ground. This modification does not alter the basic action of the oscillator but causes a more linear discharge rate of C_3, permitting very accurate control of the oscillator. For explanation purposes, it could be assumed that point "A" is grounded. The oscillator would then be identical to the circuit of Figure 2 and the same explanations would hold.

The circuit of Figure 4 employs the same blocking oscillator as does Figure 1. However, the method of coupling the trigger pulses from the master oscillator to the "÷15" divider is considerably different. In the plate circuit of V_1, the positive pulses are taken from the primary winding of transformer T_1 and coupled through

C_2, CR_1, R_5, T_2 and C_3 to the grid of V_2. CR_1 is connected so that a positive pulse at the junction of C_2-R_4 causes the diode to conduct thus permitting pulses to be fed from the master oscillator to the "÷15" oscillator.

In order to prevent any pulses in the V_2 grid from being fed back to the master oscillator plate circuit, and affecting the frequency of the master oscillator, CR_2 is connected so that the negative pulses are shorted to ground. CR_1 can conduct only when its left hand electrode is positive and presents an open circuit to any positive pulses that are applied to its right hand electrode. Thus, the combination of CR_1 and CR_2 functions as a one-way gate to permit pulses to pass from V_1 to V_2 but does not permit passage of pulses from V_2 to V_1.

The pulses in the cathode of V_2 are of positive polarity with a frequency of 31.5 kc divided by 15 or 2.1 kc. These pulses are then coupled to the grid of the next divider in the timer. Diodes CR_3 and CR_4 perform the same duties as CR_1 and CR_2.

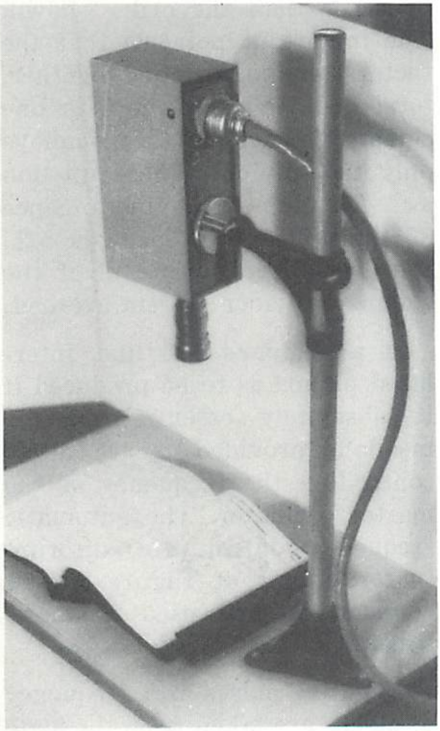
Adjustment of the master oscillator frequency is made by placing an oscilloscope at the "divide by 15" test point and varying R_3 and R_8 so that V_2 conducts on every fifteenth pulse.

Afc Discriminator

As previously mentioned, the output of the 31.5 kc master oscillator is carried through a series of dividers to obtain a 60 cps pulse that is used to control the vertical deflection circuits. There are usually four divider stages that divide the master oscillator frequency by factors of seven, five, five, and three. The order of this division is not important and may be other than the order shown. The important point is that the factors, when multiplied together, total 525. In fact, there is one commercial system that employs only two dividers that function as ÷25 and ÷21 dividers. Since 25 multiplied by 21 equals 525, the over-all requirements of the complete divider system are met.

If a standard 525 line, interlaced picture is to be produced it is absolutely essential that a means be provided for accurately controlling the frequency of the master oscillator. The automatic frequency control (afc) discriminator circuit of Figure 5 is a common method used in many timers.

Negative pulses at a frequency of 60 cps are taken from the plate circuit of the last divider and fed through C_1 and C_3 to CR_1. Since the electron flow through a crystal diode is always against the arrow symbol, electrons pass down through CR_1, down through C_5 to ground, through the source of the pulses to C_1 and finally back to C_3. This action charges the ungrounded plate of C_5 negative and also charges C_3 to the polarity shown. During the time between pulses, C_3 discharges through R_2, R_4 and R_5. R_5, being much greater in resistance than R_2 or R_4, has practically all of the voltage developed across it and the polarity is as shown.



Transmission of data concerning the production of products in a metal factory. The information is being observed on a distant monitor.
Courtesy Kay Laboratories

At the same time that the negative pulses are being applied to CR_1, positive pulses are applied to CR_2 and it conducts through C_4, C_2, the source of the pulses to ground, and through C_5. The charge across C_5 is such that its ungrounded plate is positive and the charge across C_4 is as shown. Between positive pulses, C_4 discharges through R_6, R_4 and R_3 back to the left plate of the capacitor. This electron flow develops a voltage across R_6 as indicated.

When the pulses are first applied to the circuit, C_1 and C_2 charge to the same voltage as C_3 and C_4. During the time that the pulses are not causing conduction of the crystal diodes, C_1 completely discharges through R_2, and C_2 completely discharges through R_3 as the C_1R_2 combination and the C_2R_3 combination have short RC time constants in respect to the time of one cycle of the input pulses. On the other hand, the C_3R_5 and C_4R_6 combinations have long time constants in comparison to the time of one cycle of the input pulses. C_3 and C_4 thus are prevented from discharging rapidly and they retain most of their charge until the next pulse causes conduction of the diodes and recharges them.

After a number of cycles have occurred, capacitors C_3 and C_4 charge to almost the peak of the applied pulses while capacitors C_1 and C_2 have very *little charge.* The reason for this rather unusual occurrence can best be explained by analyzing the drawings of Figure 6.

In Figure 6A we have shown two equal capacitors in series with switch S_1 and a 100 volt battery. Switch S_2 is in parallel with C_2 only. In Figure 6B we have closed S_1 and left S_2 open which charges the capacitors to the full battery voltage. Being equal in value, C_1 and C_2 each charge to 50 volts. In Figure 6C, we have opened switch S_1 which removes the battery from the circuit and closed switch S_2 which permits C_2 to completely discharge while C_1 retains its charge of 50 volts. Since C_1 has a charge of 50 volts and C_2 has a charge of zero volts, the total capacitor voltage is 50 volts.

Now, in continuous pulsing or switching circuits such as indicated in Figure 6, it is a characteristic of two equal capacitors in series that the difference in potential between the source voltage and the previously charged capacitor voltage will always divide up equally between the two capacitors. In Figure 6D we have once again opened S_2 and closed S_1 so that the difference between the battery voltage and the total capacitor voltage will divide equally. Half of this difference, $(100-50)\div 2$ or 25 volts, adds to the charge on C_1 and the remaining 25 volts charges C_2 so that C_1 is charged to 75 volts and C_2 charged to 25 volts; the total of which is still equal to the 100 volts of the battery.

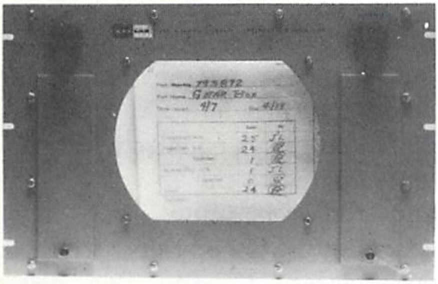
In Figure 6E we repeat the procedure of opening S_1 and closing S_2 which discharges C_2 completely but C_1 retains its charge of 75 volts.

Finally, in Figure 6F we have again opened S_2 and closed S_1. Since the difference in potential between the battery and the charge on C_1 is now 25 volts, this 25 volts divides equally with 12.5 volts adding to the 75 volts on C_1 and the remaining 12.5 volts charging C_2. We end up with 87.5 volts across C_1 and 12.5 volts across C_2.

This procedure can be followed until C_1 is charged to practically the full battery voltage and C_2 has almost no charge at all.

Getting back to the circuit of Figure 5, this switching action is performed automatically by the pulses and the net result is that C_3 and C_4 are charged to the peak of the pulses while C_1 and C_2 have very little charge. The voltage developed across R_5 and R_6, due to the fact that C_3 and C_4 are attempting to discharge, places a bias on CR_1 and CR_2 and permits them to conduct only on the peaks of the input pulses.

C_5 is considerably larger than C_3 or C_4 and will have a small charge across it when the crystal diodes conduct. The charge across C_5 due to the conduction of CR_1 will be exactly opposite in polarity to the charge developed across it due to the conduction of CR_2. Therefore, as long as the two diodes conduct equally, the charge across C_5 is zero.



Reception of the data transmitted by the camera in the previous photograph.
Courtesy Kay Laboratories

The 6.3 v a-c sine wave is applied to the voltage divider consisting of R_1 and R_4. This divider reduces the 60 cps sine wave to the proper amplitude since the pulses applied to the discriminator are approximately 6 volts peak-to-peak and they should be about twice the amplitude of the sine wave if the circuit is to function normally.

The pulses and the sine wave are applied to the crystal diodes and their difference in conduction determines the amplitude and polarity of the voltage developed across C_5. Figures 7 and 8 are graphical representations of the manner in which this change of voltage is accomplished.

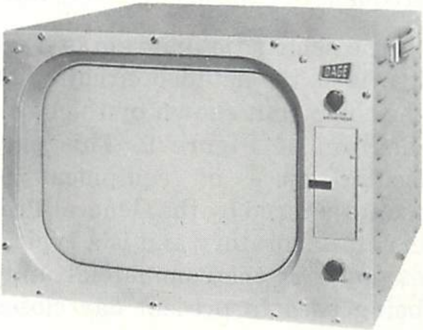
Figure 7A shows the negative pulses that are applied through C_1 and C_3 causing conduction of CR_1. Figure 7B indicates the sine wave that is applied to the same diode. Figures 8A and 8B show the positive pulses and the sine wave respectively that cause conduction of CR_2. When the frequency and phase of the master oscillator is correct, the pulses in the output of the last divider occur at exactly the instant of time when the sine wave is passing through zero as indicated in Figures 7C and 8C. In this case, the-peak-to peak amplitude of the combination voltage applied to each diode is the same and the diodes conduct equally resulting in no change of voltage across C_5.

If, for any reason, the frequency of the master oscillator increases slightly, the negative pulses applied to CR_1 occur when the sine wave is positive as shown in Figure 7D. The peak-to -peak amplitude of this combination is less than that of Figure 7C and CR_1 accordingly reduces its conduction. At the same time, the positive pulses applied to CR_2 also occur when the sine wave is positive as shown in Figure 8D.

However, the peak-to-peak amplitude of this combination is greater than that of Figure 8C and CR_2 increases its conduction. As previously explained, this condition causes a charge developed across C_5 so that its ungrounded plate is positive. This positive direct voltage is applied to the grid of V_1 which—functioning as a d-c amplifier — amplifies this change and causes the voltage at its plate to become less positive. The voltage at the plate of V_1 is, in turn, used as the B+ voltage to which the grid of the master oscillator is returned (Point "A" of Figure 1). With a less positive voltage applied to the grid return circuits, the grid becomes more negative and the oscillations slow down, thus returning the master oscillator to its correct frequency.

If the frequency of the master oscillator decreases slightly, the pulses occur after the sine wave passes through zero. As shown in Figure 7E, this causes the peak to peak voltage applied to CR_1 to increase which increases its conduction. At the same time, Figure 8E shows that the total voltage applied to CR_2 has reduced. Under these conditions, the voltage developed across C_5 causes the grid of V_1 to become negative in respect to ground resulting in a corresponding increase in the plate voltage of V_1. This increase of V_1 plate voltage causes the frequency of the master oscillator to increase bringing it back to normal.

Summing up the entire action of Figure 5 briefly, an increase in the master oscillator frequency will cause an increase in conduction of CR_2 and a decrease in conduction of CR_1. The resultant voltage across C_5 will be positive and, after being amplified by V_1, allows the master oscillator to slow down. A decrease in the master oscillator frequency causes an increase in conduction of CR_1 and a decrease in conduction of CR_2. The voltage developed across C_5 will be negative and will result in the master oscillator being speeded up.



This monitor has provision for separate sync insertion and can be used for broadcast as well as closed circuit TV.

Courtesy Dage Television Division—
Thompson Products, Inc.

COMPLETE TIMER

The block diagram of a complete timer unit is shown in Figure 9. In this timer, the output of the master oscillator is fed to a divider system which employs division by three, seven, five and five. Positive and negative pulses from the last divider are fed into the afc discriminator along with the sine wave obtained from the 6.3 v a-c source. The output of the discriminator is fed to a control tube which, in turn, controls the frequency of the master oscillator.

The schematic diagram of Figure 10 is the detailed circuitry of the timer unit shown by the block diagram of Figure 9. This particular piece of equipment is manufactured by the General Precision Laboratory and is a typical example of the commercial units being used in present day closed circuit television systems.

At the left in the Figure, the triode section of the 6U8 (V_{401}) is connected as an LC oscillator with L_{401} being variable and acting as the master oscillator frequency control. The pentode section of V_{401} is a reactance tube which, in this case, is connected to act as a variable inductance.

The sine wave that is present at the plate of 6U8 pentode is applied across the series circuit of R_{402} and C_{401}. At a frequency of 15,750 cps, the reactance of the 270 $\mu\mu$f capacitor is small in comparison to the resistance of the 470 K resistor. This causes the combination to be primarily a resistive circuit and the current through the two components is in phase with the voltage at the plate of the V_{401} pentode. Since the voltage across a capacitor always lags the current through it by 90° a small portion of the pentode plate voltage is developed across C_{401} and this voltage lags the plate voltage by approximately 90°. Since the plate current of the tube is in phase with the grid voltage, the plate current also lags the plate voltage by 90°. The changes in plate voltage lead the changes in plate current by 90° and the tube is effectively an inductance.

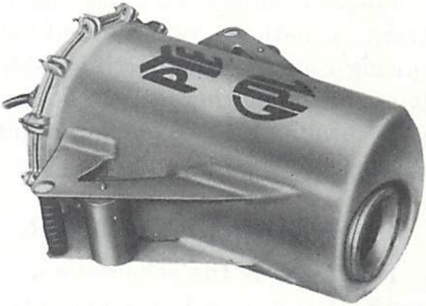
Now, in order to control the frequency of the oscillator, it is necessary to control the average conduction of the pentode reactance tube. Reducing the bias on the tube by applying a positive direct voltage to its grid will cause the average conduction to increase which represents a decrease in inductive reactance. A decrease in inductive reactance means that the inductance has decreased. Finally, since the resonant frequency of a tuned circuit is inversely proportional to the inductance $\left(f_o = \frac{1}{2\pi\sqrt{LC}}\right)$ a decrease in inductance causes an increase in resonant frequency.

Applying a negative voltage to the grid of the reactance tube reduces its conduction, increases its effective inductive reactance, increases its effective inductance and reduces the resonant frequency of the tuned circuit.

In Figure 10, the control voltage for the reactance tube section of V_{401} is obtained from the output of the afc discriminator circuit consisting of SR_{401}, SR_{402} and their associated components. When the SPST toggle switch S_{401} is placed in the "Free" position, the control voltage output from the afc system is shorted to ground and the master oscillator is free running. The master oscillator and the divider are adjusted for stable operation by the procedure described earlier in the lesson. The switch is then placed in the "Lock" position and the entire timer is synchronized with 60 cps line voltage.

To follow the overall action of the timer, the 31.5 kc signals are taken off at point 5 and fed through a connecting cable to the horizontal sweep circuits. Even though these signals are twice the frequency of the horizontal scanning rate, application of the principle previously explained for a "divide by two" divider can be used to maintain synchronization.

The 31.5 kc signals are also fed through R_{406} and CR_{407} to pin 1 of V_{402A}. CR_{407} allows only the negative portion of the sine wave to be applied to the plate and prevents the negative pulse at the plate of V_{402A} from being coupled back to the master oscillator. Variable resistor R_{436} adjusts the frequency of the "divide by three" blocking oscillator and positive pulses at a frequency of 10,500 cps are fed through C_{411}, CR_{401}, R_{412} , the secondary of T_{402} and through C_{412} to the grid of the right hand section of V_{402}. An oscilloscope can be connected to the junction of R_{412} and R_{411} to observe the waveform while adjusting R_{436}.



Underwater television camera for use in submarine engineering, channel inspection, and other similar services.

Courtesy General Precision Laboratories, Inc.

Right hand section V_{402B} is a "divide by seven" blocking oscillator which provides positive pulses at a frequency of 1500 cps at its cathode. R_{417} adjusts the free-running frequency while the wave-form at the junction of R_{414} and R_{415} is being observed on a scope. The positive pulses are then fed to the grid of V_{403A} and divided by five to provide an oscillation frequency of 300 cps. The positive pulses at the cathode are fed to the grid of V_{403B} which functions as a "divide by five" oscillator and 60 cps pulses are obtained in its output.

Negative 60 cps pulses are taken from the plate circuit at the junction of R_{427} and R_{440} while positive 60 cps pulses are taken from the cathode and applied, along with the 60 cps sine wave obtained from the power source, to the afc discriminator.

Positive pulses also are taken from the cathode, point 4, and fed through an interconnecting cable to synchronize the vertical deflection circuits of the camera and the monitor.

BLANKING GENERATOR

Figure 11 is the schematic diagram of the circuits used to form the blanking pulses from the vertical and horizontal pulses derived from the timer unit. Positive pulses at a frequency of 60 cps are fed to the grid of V_1 where they are amplified and inverted in polarity. These negative pulses are applied to the grid of V_2 and appear as positive pulses in its plate circuit.

To the grid of V_3 are applied positive horizontal pulses. Operating as a cathode follower, V_3 causes positive pulses to be developed across R_7 and coupled through C_2 to the cathode of V_2. Since positive pulses applied to the cathode have the same effect as negative pulses applied to the grid, positive horizontal pulses appear in the plate circuit of V_2 along with the positive vertical pulses.

Unless some arrangement is made to prevent it, the horizontal pulses that occur during the vertical blanking pulse period would ride on top of the vertical blanking pulses. Therefore, the value of resistors R_5 and R_6 are chosen so that the most negative portion of the pulses applied to the grid of V_2 cause the tube to be cut off. Then, when the positive horizontal pulses are applied to the cathode they drive tube V_2 still further beyond cutoff and are eliminated from the composite blanking signal in the plate circuit. It should be remembered, that this situation occurs only during the periods of time when the vertical and horizontal pulses are applied simultaneously. During the long intervals of time when the vertical pulses are not present on the grid of V_2, the horizontal pulses applied to its cathode permit it to be driven just far enough beyond cutoff so that only the peaks are clipped. Thus, the output in the plate circuit of V_2 is positive blanking pulses with flat tops.

The composite blanking signal is coupled through C_3 and CR_1 to the grid of V_4 where it is amplified and appears as negative blanking pulses. Notice that C_3 and C_5

have polarity markings indicating that they are electrolytic capacitors. In order to prevent the vertical blanking pulses from becoming differentiated, a very long RC time constant must be employed. The most practical way to do this is to use large values of capacitance. Therefore, electrolytics are chosen.

Since the output of V_2 consists of flat-topped positive pulses, it is now merely necessary to "square off" the negative alternation of the pulse cycle in order for them to have the proper shape. When the pulses are applied to CR_1 the positive portion causes conduction of the diode and a corresponding voltage is developed across R_{10} without attenuation. Since CR_1 does not conduct on the negative alternation, any irregularities in this negative portion of the blanking signal are effectively removed.

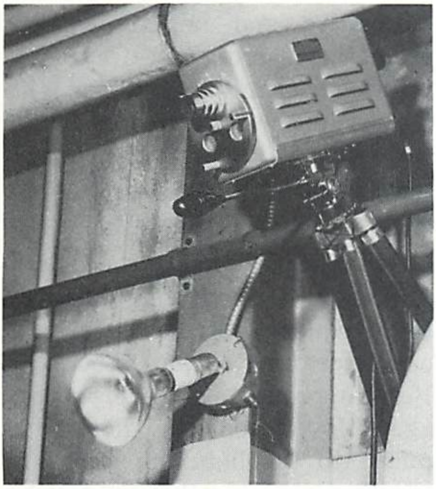
COMPLETE CAMERA CONTROL

The block diagram of Figure 12 is that of a CAMERA CONTROL UNIT manufactured by the Diamond Power Specialty Corporation and used in conjunction with their "Utilivue" camera chain. Starting with the master oscillator, V_{109B}, the 31.5 kilocycle signal is fed through a "divide by 3" divider to produce pulses at a frequency of 10,500 cps; through a "divide by five" divider the output of which is 2,100 cps pulses; through a "divide by seven" divider to produce 300 cps pulses; through a "divide by five" divider to produce 60 cps pulses.

Positive and negative pulses from the last divider are fed to an afc discriminator, along with 60 cps line voltage, to produce a d-c output voltage which is amplified and used to control the master oscillator and the dividers.

The 31.5 kilocycle signal is amplified by V_{110} and used to control the frequency of the horizontal oscillator and output tube V_{111}. Besides producing the high voltage, V_{111} feeds the horizontal pulses to the blanking and sync amplifier, V_{102}. In this same stage is added the vertical pulses obtained from the vertical oscillator and amplifier V_{106}. The output of V_{102} is fed to the blanking amplifier in the camera and to a delay line where the signals are delayed sufficiently to be used as sync pulses. Then, the pulses are added to the video signal in the third video amplifier, V_{104}.

From the camera pre-amplifier, the video signal is fed through a channel limiter which limits both the positive and negative peaks of the signal. After being amplified by the second video amplifier, the video signal is mixed with the sync pulses and further amplified in V_{104}. The complete composite signal is then fed to V_{105} which is a cathode follower and develops the signal across a low resistance in its cathode circuit. From here, the signal is then fed by coaxial cable to the monitor.



Camera mounted temporarily to observe the action of some heavy machinery.
Courtesy Allen B. DuMont Laboratories, Inc.

The complete composite signal is fed from the plate circuit of V_{105} to the V_{114} stage which is the r-f transmitter. Accordingly, a modulated r-f signal, as well as the composite video signal is available and can be fed by coaxial cable or twin lead to a TV receiver.

Power Supply

As shown in the schematic diagram of Figure 13, the power supply for this camera control unit contains two identical constant-voltage transformers with their "matching" windings wired in parallel. The use of constant-voltage transformers prevents line voltage variations, within the operating limits of the transformers, from affecting the output of the power supply. The use of two transformers instead of one with higher current ratings is due to space restrictions. Since this particular control unit is mounted as a part of the camera, the unit is designed as compact as possible. This same space restriction necessitated the use of a 5U4GA type rectifier tube in place of the 5U4G as the former has the same ratings but is smaller in diameter.

The 100 ohm, 10 watt resistor in series with the center taps of the transformer secondaries is used to reduce the d-c output of the power supply to the voltage that is required by the various circuits. The neon bulb that is in series with R_{206} is the ON-OFF indicator and glows when the power switch, S_{101}, is closed.

Timer

This complete camera chain is designed to provide 525 line, 60 field, 30 frame television pictures. Therefore, it is necessary to include a controlled timer. As indicated in the lower right portion of Figure 13, this timer employs three dual triode tubes which are V_{109A} and $_B$, V_{108A} and $_B$, and V_{107A} and $_B$. (As a point of clarification, the section of the double triode tubes using pins 1, 2, and 3 are the "A" sections and the section using pins 6, 7, and 8 are the "B" sections.) The timer also includes an afc system and a 3 pole, 3 position switch S_{102}.

V_{109B} is the master oscillator and operates at a frequency of 31.5 kc. As a blocking oscillator, its free-running frequency is determined by the RC network in its grid circuit which consists of a 120 $\mu\mu$f capacitor (C_{153}), a 390 K ohm fixed resistor (R_{195}), and a 250 K ohm variable resistor (R_{194}). This 250 K ohm variable resistor is the master oscillator frequency control. Also connected to the grid of V_{109B} is a 68 $\mu\mu$f capacitor (C_{152}) which is in series with a 10 K ohm resistor connected to ground. The junction of these two components is brought out and made accessible as an oscilloscope test point. The purpose of this network is to provide a convenient means of observing the wave-form at the grid of the oscillator without having the frequency of the oscillator affected when a scope lead is connected to it.

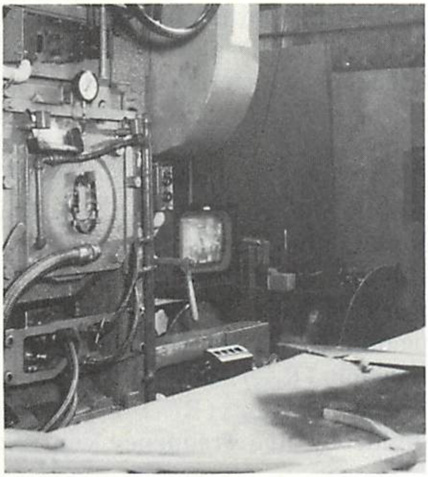
A portion of this 31.5 kc signal is taken from the plate circuit of V_{109B} and fed through a 22 $\mu\mu$f capacitor (C_{151}) to the grid of V_{109A} which is another blocking oscillator driven by the 31.5 kc signal applied to its grid. The free-running frequency of this oscillator is one third that of the master oscillator or 10,500 cps. The circuit time constant is determined by the 330 $\mu\mu$f capacitor (C_{149}) and a combination of the 390 K ohm fixed resistance (R_{190}) in series with a variable resistance of 250 K ohms (R_{191}). This component selection affects a division by three and R_{191} is the divide by three frequency control.

V_{108B} is another blocking oscillator operating at a frequency of 2100 cps which is one-fifth that of the divide by three stage. This stage is driven by a portion of the 10,500 cps signal fed through a 22 K ohm resistor (R_{189}) which couples the plates of the two oscillators. The time constant network consists of the .001 μf capacitor (C_{148}), the 1 megohm fixed resistor (R_{188}), and the variable 500 K resistor (R_{187}) being the divide by five frequency control.

A portion of the 2100 cps signal is coupled from the plate of V_{108B} through an 18 K resistor (R_{184}) to the plate of V_{108A}. The free-running frequency of this blocking oscillator is 300 cps or one-seventh of the 2100 cps oscillator. C_{145}, R_{182}, and R_{183} determine this frequency with R_{183} being the divide by seven frequency control.

The 300 cycle signal is fed to the plate of V_{107B} through R_{181} and drives this final divider which operates at a frequency of 60 cps.

C_{142}, R_{176}, and R_{177} are chosen so that a division by five is obtained. Thus the master oscillator frequency is divided by three, five, seven, and five. These factors multiplied together give a product of 525 and since these oscillators are all "locked" together, the highest frequency (31.5 kc) is always exactly 525 times the lowest frequency of 60 cps.



Machinery operation being monitored at the site of additional equipment.
Courtesy Allen B. DuMont Laboratories, Inc.

It should be noticed that the manner of feeding the driving signal from one divider to the next oscillator is different in the case of coupling the master oscillator to the first divider stage. The reason for capacitive coupling is to isolate the master oscillator from the rest of the divider chain. Also, each stage has a corresponding test point at which scope observations can be made.

Another point of considerable interest is the relationship of the RC time constants in the grid circuits of succeeding oscillators. The master oscillator RC time constant is approximately 77 microseconds, the RC time constant of the divide by three divider is about 210 microseconds, that of the divide by five divider is about 1500 microseconds, that of the divide by seven divider is about 17000 microseconds and that of the final divide by five divider is about 35000 microseconds.

Even though the maximum time constant of each successive oscillator is not the exact multiple by which it divides, the various frequency controls can be adjusted so that proper frequency division is obtained.

At the end of the chain, a positive pulse from the cathode and a negative pulse from the plate circuit are derived from the 60 cycle oscillator. These pulses are of equal amplitude and are fed into a phase comparison network along with the 6.3 v a-c signal which is obtained from the 60 cycle power source through the power transformer.

The output of the afc discriminator or phase comparator is a direct voltage that varies either positive, negative, or zero in accordance with the phase relationship of the two timer pulses to that of the 60 cycle line. If the timer pulses are at the same frequency as the 60 cycle line voltage the direct voltage output of the afc circuit is zero. If the timer pulses increase in frequency, the resultant output is a positive voltage that is proportional to the frequency increase. If the timer pulses decrease in frequency, the resultant is a proportional negative voltage.

The output of the afc discriminator is filtered and applied to the grid of V_{107A} which is a d-c amplifier. A 33 K ohm resistor (R_{169}) is the plate load and the plate end of this resistor is connected to the grid return circuits of all the oscillators. Any change in the output of the afc discriminator causes the conduction of the tube to vary which changes the plate voltage of V_{107A} and the grid voltage of the oscillators.

If the pulses in the output of the timer are too high in frequency, a positive voltage is applied to the grid of the d-c amplifier which causes the grids of the oscillators to become more negative. This causes the blocking capacitors in these grid circuits to take more time to discharge and decreases the frequency of the oscillators to bring them back in phase with the 60 cycle line. If the pulses in the output of the timer decrease in frequency, the voltage applied to the grid of V_{107A} is negative which causes the oscillator grids to swing more positive and their frequency is increased.

Selection by the three pole three position switch S_{102}, allows the timer to be free-running, (position #1) ; to be locked to the 60 cycle line (position #2), or to be cut out of the circuit entirely (position #3).

Section A of this switch provides B+ for the timer and, in the timer out position #3, a resistance load replaces the timer d-c circuit to provide a constant current drain on the power supply. This arrangement prevents defocusing of the picture when the timer is not in the circuit.

Section B feeds the 60 cps pulses from the last divider to drive the vertical oscillator tube V_{106A}. When the timer is out of the circuit (position #3), the switch feeds a 6.3 v a-c line signal to drive the vertical oscillator.

Section C grounds the grid of d-c amplifier V_{107A} when the timer is free-running. This free-running position is necessary so that no correction voltages are fed back when setting up the timer.

In the timer free-running position, the horizontal and vertical sweep circuits are locked together but are not locked with the line. In the timer locked position the horizontal and vertical are locked together and also locked with the line frequency. In the timer out position, the vertical oscillator is locked to the line but the horizontal oscillator is free-running.

Vertical Deflection

V_{106A} is a blocking oscillator used to develop the vertical scanning voltage and the pulses for vertical blanking. The frequency range of this driven oscillator is such that it can be locked by either the 60 cycle line or by the 60 cycle pulses from the timer. Consequently a vertical frequency control is not required.

The circuits of V_{106B} comprise the vertical amplifier wherein height control R_{149} determines the amount of signal fed to its grid, and control R_{150} in the cathode circuit varies the vertical linearity. One side of the secondary of the vertical output transformer T_{102} is connected to the movable arm of the vertical centering control R_{157} which is in series with B+. The other side of the secondary is connected through the vertical deflection coils (lugs 14 and 6 of plug P_{101}) to the fixed tap on the centering control. This method permits the amplitude and polarity of the direct current through the deflection coils to be varied and provide the centering action.

Horizontal Deflection and High Voltage

The 31.5 kc pulses are also developed across R_{196} in the plate circuit of V_{109B} and connected to T_{26} on the terminal strip. From this point the pulses are fed through C_{120} to the grid of V_{110A}. This tube and V_{110B} are amplifiers which increase the amplitude of the pulses sufficiently to synchronize V_{111}, the horizontal oscillator, with the master timer oscillator. The resonant frequency of V_{111} is 15,750 cps which effects a division by two of the master oscillator. In this way, the necessary timing sequence for interlaced scanning is obtained.

A portion of the 15,750 cps sawtooth wave-form on the screen grid of V_{111} is fed back to the control grid of V_{110B}. This sawtooth voltage gates the grid of V_{110B} so that only every second pulse of the 31.5 kc input signal appears in the V_{110B} plate circuit.

The horizontal oscillator is a "Beam Relaxor" circuit which furnishes deflection power, blanking pulses, and high voltage pulses to the high voltage rectifier. The frequency determining circuit of this oscillator is due to an RL time constant rather than an RC time constant. The inductance of transformer T_{101} works in conjunction with the plate resistance (R_p) of the tube, and the resistance in the cathode circuit. The resistance in the cathode is made up of the 300 ohm potentiometer R_{139} which is the frequency control and the 50 ohm center tapped potentiometer which is the horizontal centering control. Both the center tap and the movable arm are by-passed by 40 μf capacitors C_{114} and C_{115} which filter any variation of voltage due to the changing current of V_{111} and maintain a constant voltage between these points and ground. The horizontal deflection coils are connected across these two points (through pins 7 and 15 of plug P_{101}) and centering is accomplished.

The high voltage transformer T_{101} secondary feeds high voltage pulses to rectifiers V_{112} and V_{113}. These tubes are connected in parallel to provide sufficient current. The filtered output of these rectifiers provides a negative voltage of about 2700 volts which is fed to pin #13 of P_{101} and then to the camera chassis.

Blanking and Sync Generation

Negative horizontal pulses are fed from the control grid of V_{111} to the control grid of the left triode section of V_{102}, at the upper left in the diagram. The small capacitor C_{101}, connected between grid and ground, makes the pulses the proper width for blanking. The grid load consists of two crystal diodes CR_{101} and CR_{102} which clamp the pulses to a ground reference. When the negative portion of the horizontal pulses occurs, the two diodes do not conduct and permit the pulses to drive the tube into cutoff. When the positive portion of the pulses occur, both diodes conduct and short the grid to ground which provides the clamping action.

Negative vertical pulses are applied to the junction of the two diodes. During the negative portion of these pulses, CR_{101} conducts and applies the pulses to the left grid of V_{102}. During the positive portion of these pulses, CR_{102} conducts and shorts the pulses to ground. The resultant wave-forms on the plate and cathode of the left triode of V_{102} are mixed positive blanking pulses that are clipped to the proper amplitude.

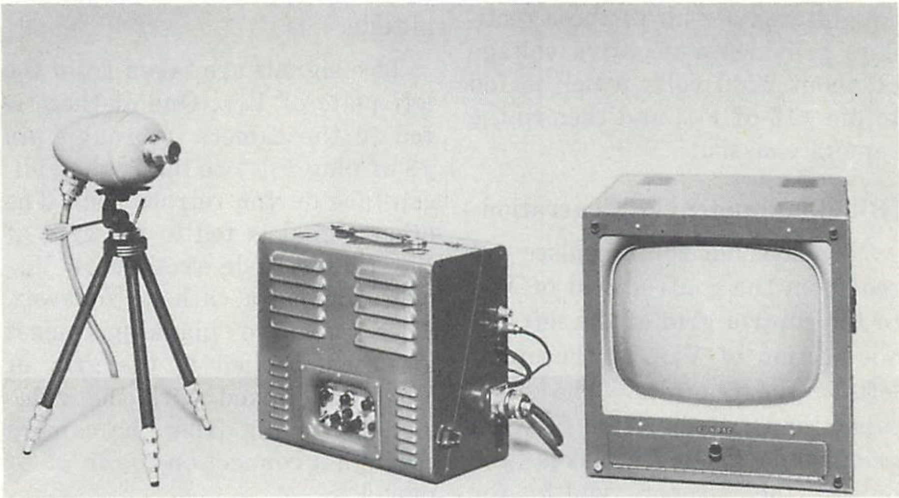
Two signals are taken from the left plate of V_{102}. One of these is fed to the camera (through pin #8 of plug P_{101}) to blank the vidicon tube during retrace time. The other signal is fed to the grid of the right triode section of V_{102} operating as a cathode follower. These positive blanking pulses are then applied to the grid of V_{103A} and mixed with the video signal arriving from the camera through a connection to pin #1 of plug P_{101}.

Negative blanking pulses on the cathode of V_{102A} are fed to a lumped transmission line type of delay line (L_{101} to L_{107} and C_{164} to C_{170}). This delay line narrows the pulses and delays them sufficiently so that they can be used as synchronizing pulses. When they are reinserted at the cathode of V_{104}, they mix with the blanking pulses and the proper "front porch" of the composite signal will have been established.

Video Amplifier Circuits

As mentioned, the negatively polarized video (negative picture phase) signal arriving from the camera is mixed with the positive blanking pulses on the grid of V_{103A}.

The plate circuit of V_{103A} includes a rather interesting combination of diodes and resistor networks. In parallel with the tube plate circuit is a bleeder network consisting of R_{109} and R_{110}. The latter unit is variable so that the plate voltage of V_{103A} can be adjusted to provide the proper action as will be described. Another bleeder network is connected in parallel with the B+ supply and these resistors include R_{116}, R_{115}, and R_{111}. This bleeder provides a positive voltage at the junction of resistors R_{112}, R_{111}, and R_{114} which is slightly lower in value than the positive voltage at the plate of V_{103A}. Therefore, when no signal is present in the V_{103A} plate circuit, CR_{103} does NOT conduct because its cathode is more positive than its plate. However, CR_{104} conducts and causes the top end of R_{114} to be slightly positive in respect to its lower end.



Another complete closed circuit TV system. The camera is exceptionally small and compact.
Courtesy General Precision Laboratories, Inc.

With a signal applied to the grid of V_{103A}, the composite blanking and video information in its plate circuit will be *positively polarized*, meaning that the pulses will be in a negative direction. When these negative pulses reach an amplitude sufficient to cause the cathode of CR_{103} to be negative in respect to its plate, it conducts and shorts out any portion of the signal with greater amplitude.

Since the plate of CR_{104} is positive with respect to its cathode, it will continue to conduct until the amplitude of the negative pulses causes the plate to become negative with respect to its cathode. CR_{104} will cease conducting at the same time that CR_{103} starts conducting. In this way a double clipper action exists that prevents the signal developed across L_{108} and R_{114} from going beyond a predetermined amplitude in the negative direction.

The negative portion of these pulses causes CR_{105} to conduct through L_{109}, C_{106}, and R_{117} but the positive portion of the pulses causes the cathode of CR_{105} to become positive in respect to its plate and it ceases to conduct which limits the positive peaks of the signal. The direct voltage across C_{106}, due to the conduction of CR_{105} places a positive voltage on the plate of CR_{106}. However, the voltage divider of R_{116}, R_{115}, and R_{111} places a slightly more positive voltage on the cathode of CR_{106} which prevents it from conducting during the negative and slightly positive portions of the signal. If the signal should become sufficiently positive, CR_{106} will conduct and place the 560 ohm resistor, R_{115} in parallel with L_{108} and R_{114}. This action will also limit the positive peaks of the applied signal.

To sum up the entire V_{103A} plate circuit, the four diodes form a channel through which the signal must pass. The negative limit is set by CR_{103} and CR_{104} and the positive limit is set by CR_{105} and CR_{106}. In this way, the channel limits are such that just enough signal passes through and the proper ratio of video to sync signal (which is inserted in V_{104}) is maintained. This ratio of video to sync is necessary to prevent "squashing" the sync pulses when an unusually bright object is being observed.

After being amplified by V_{103B}, which is a straight video amplifier the video and blanking signal is fed to the grid of V_{104}. Applied to the cathode of V_{104} are the negative sync pulses from the delay line. The negative sync pulses on the cathode and the positive blanking pulses and video signal on the grid are mixed in V_{104} and appear in its plate circuit as a complete composite signal with the pulses having negative polarity.

CR_{107}, in the grid circuit of V_{104}, conducts on the most positive peaks of the input signal and charges C_{108} negative on its grid side. This action further limits the positive peaks of the signal but more important—it sets a reference level so that the sync pulses mix properly with the blanking and video signal.

The composite signal is now fed to the grid of V_{105A} and $_{B}$ which is a cathode follower. The output is taken from the cathodes and provides a positively polarized composite video signal (negative going pulses) to J_{101} which is a coaxial cable jack used to feed the monitor. In the plate circuit of V_{105B}, a negatively polarized signal is developed and fed through pin #8 of J_{103} to the r-f transmitter unit.

If a coaxial cable is not connected to J_{101} with the proper load termination at the other end, a 100 ohm dummy load resistor should be used so that it parallels R_{130} and presents the proper load to the tube.

The R-F Unit

In this particular piece of equipment, the r-f unit is a completely self-contained plug-in unit deriving only filament voltage, B+, and video from the main chassis. It utilizes only two tubes contained in a single envelope, V_{114A} and $_{B}$.

V_{114B} is the oscillator section which has a frequency range such that it tunes from channel 2 through channel 6 by adjusting C_{158}. The r-f signal is electron coupled to the plate and fed through C_{160} to the cathode of V_{114B}. The composite video signal is applied to the grid of V_{114B} from pin #8 of P_{103} and modulates the r-f carrier. Then,. the modulated carrier on the plate is fed to pin #9 of P_{103}, to pin #9 of J_{103} and finally to the coaxial cable connector J_{102}. This signal can now be applied to the antenna input terminals of an ordinary TV receiver which is to be used as a monitor.

The next lesson describes some of the monitors' and accessories that may be employed in closed circuit television services.

IMPORTANT DEFINITIONS

CAMERA CONTROL UNIT—One unit of a camera chain which usually contains the sync generator and most of the controls for the camera. The actual functions will vary depending upon the manufacturer.

DIVIDERS—A circuit designed to give pulses in its output which are a sub-multiple of the frequency of the input circuit. For example, a blocking oscillator can be designed so that it will trigger on every fifth input pulse. In this case, it would be called a "divide by five" divider.

MASTER OSCILLATOR—The oscillator in the timer unit which controls all of the other oscillators or dividers. It usually operates at a frequency of 31.5 kilocycles. A series of dividers is used to divide 31.5 kc by 525 down to 60 cycles. A divide by two divider is generally used to produce the 15,750 cps for the horizontal system.

PHASE COMPARATOR—A circuit usually consisting of a double diode and various resistors and capacitors, that is used to compare the frequency and phase of the 60 cycle line voltage and 60 cps pulse from the divider network. A direct voltage proportional to any difference is developed to control the frequency of the master oscillator.

SYNC GENERATOR—The circuits used to control the frequency of the horizontal and vertical deflection systems of the camera and the timing of the blanking and sync pulses which are added to the video signal.

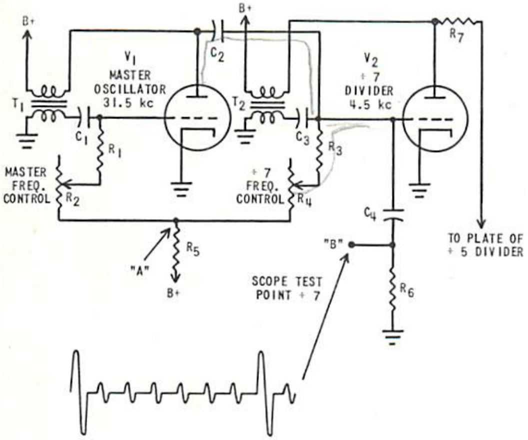


FIGURE 1

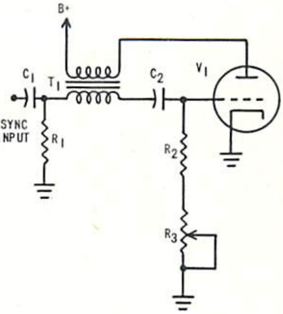


FIGURE 2

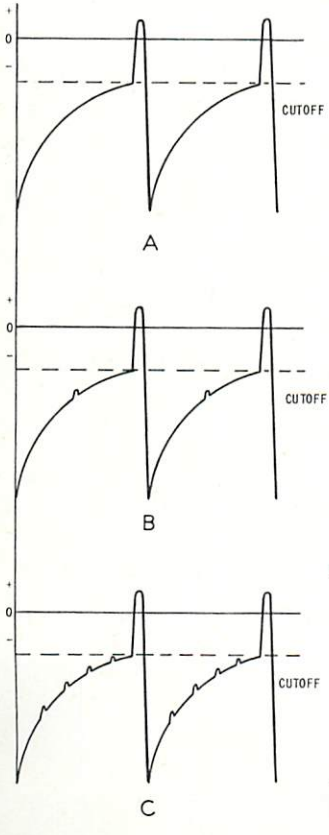


FIGURE 3

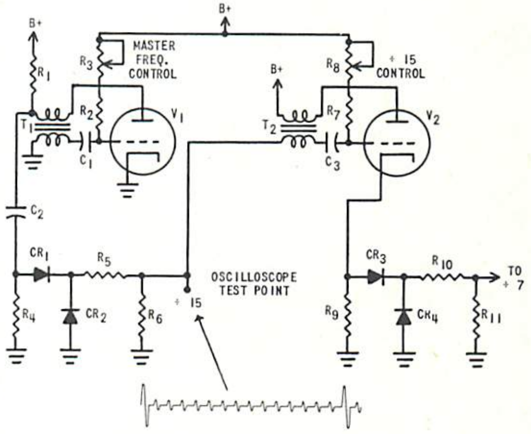


FIGURE 4

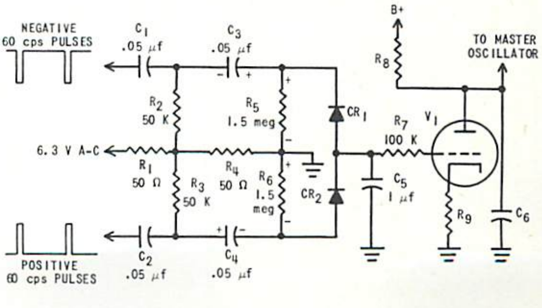


FIGURE 5

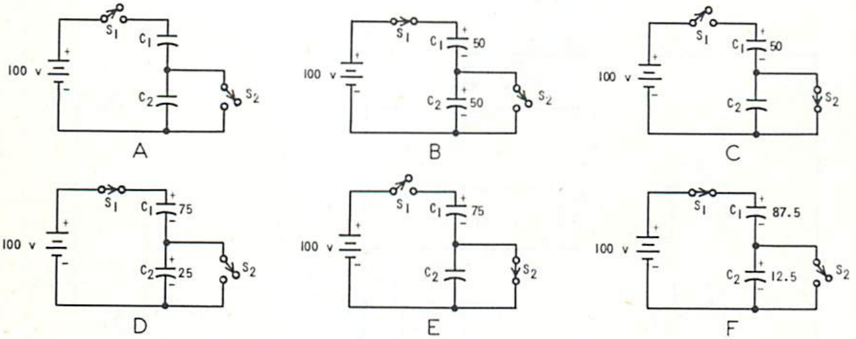


FIGURE 6

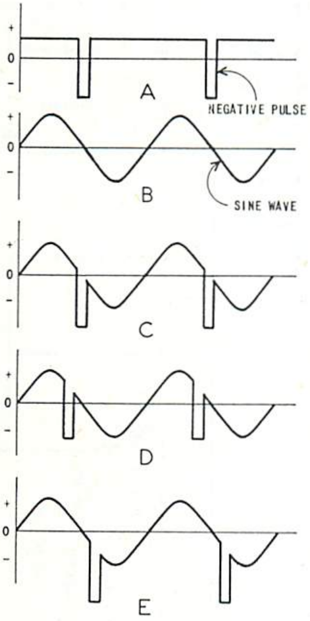


FIGURE 7

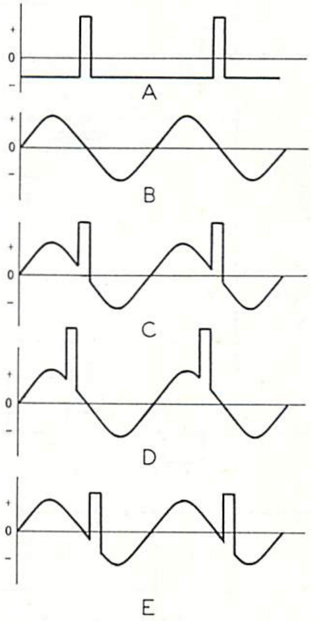


FIGURE 8

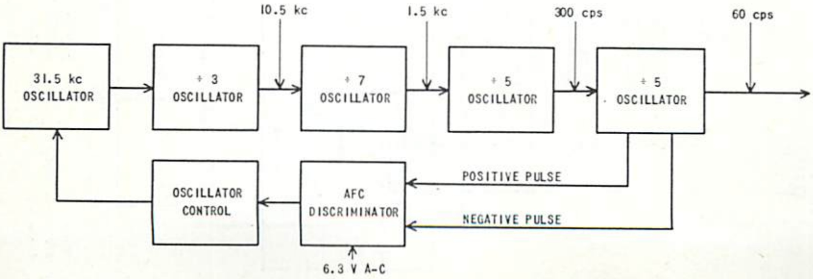


FIGURE 9

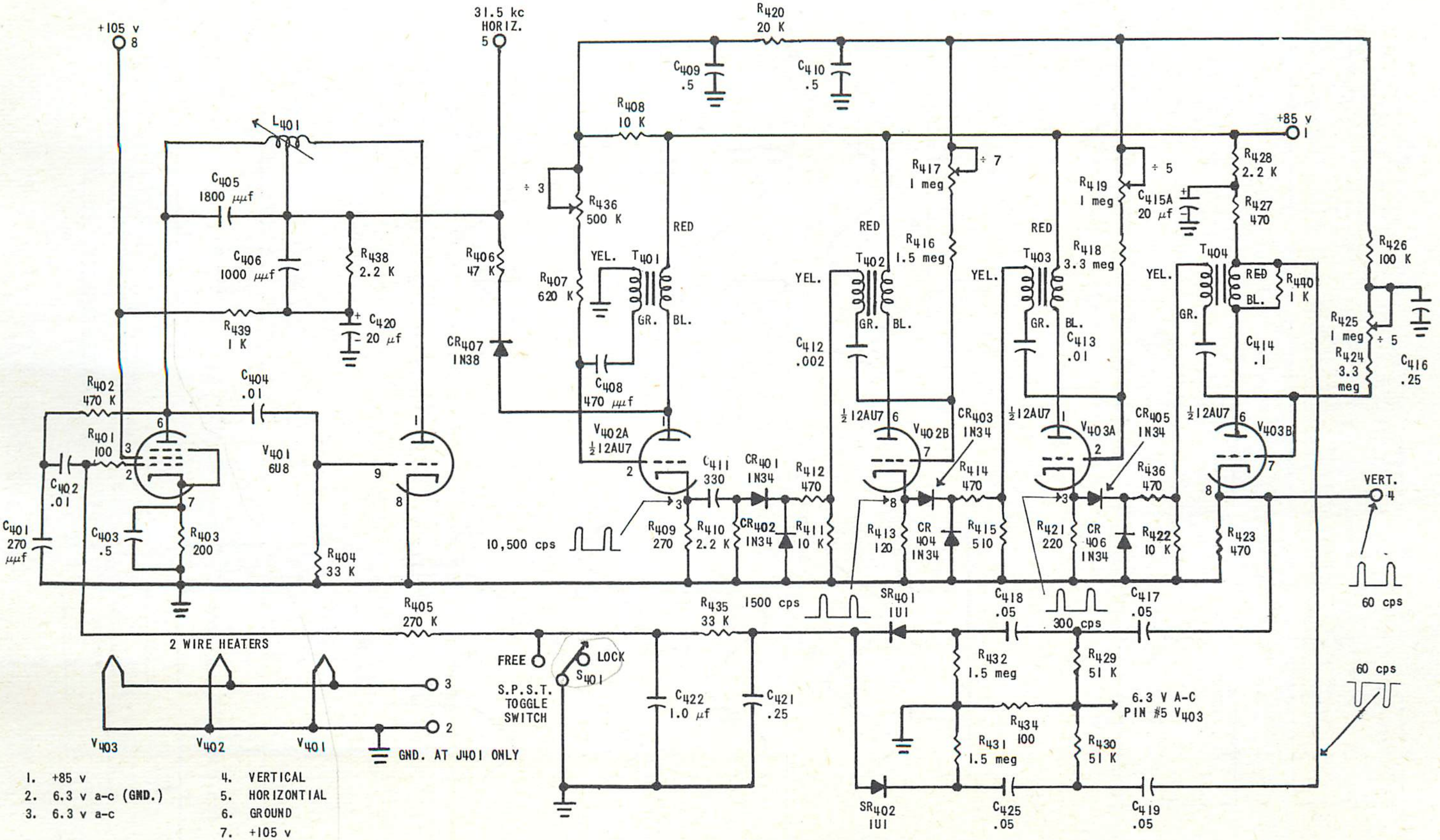


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FIGURE 10

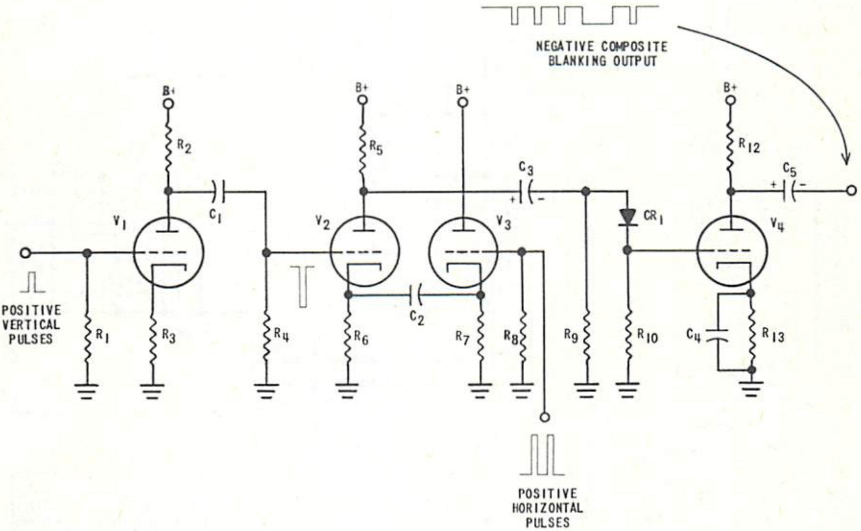


FIGURE 11

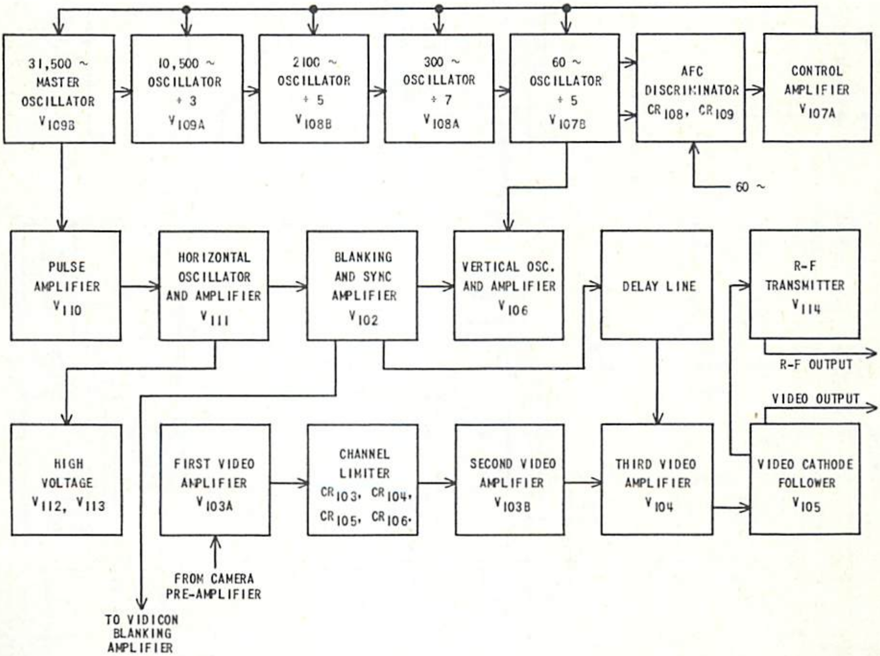
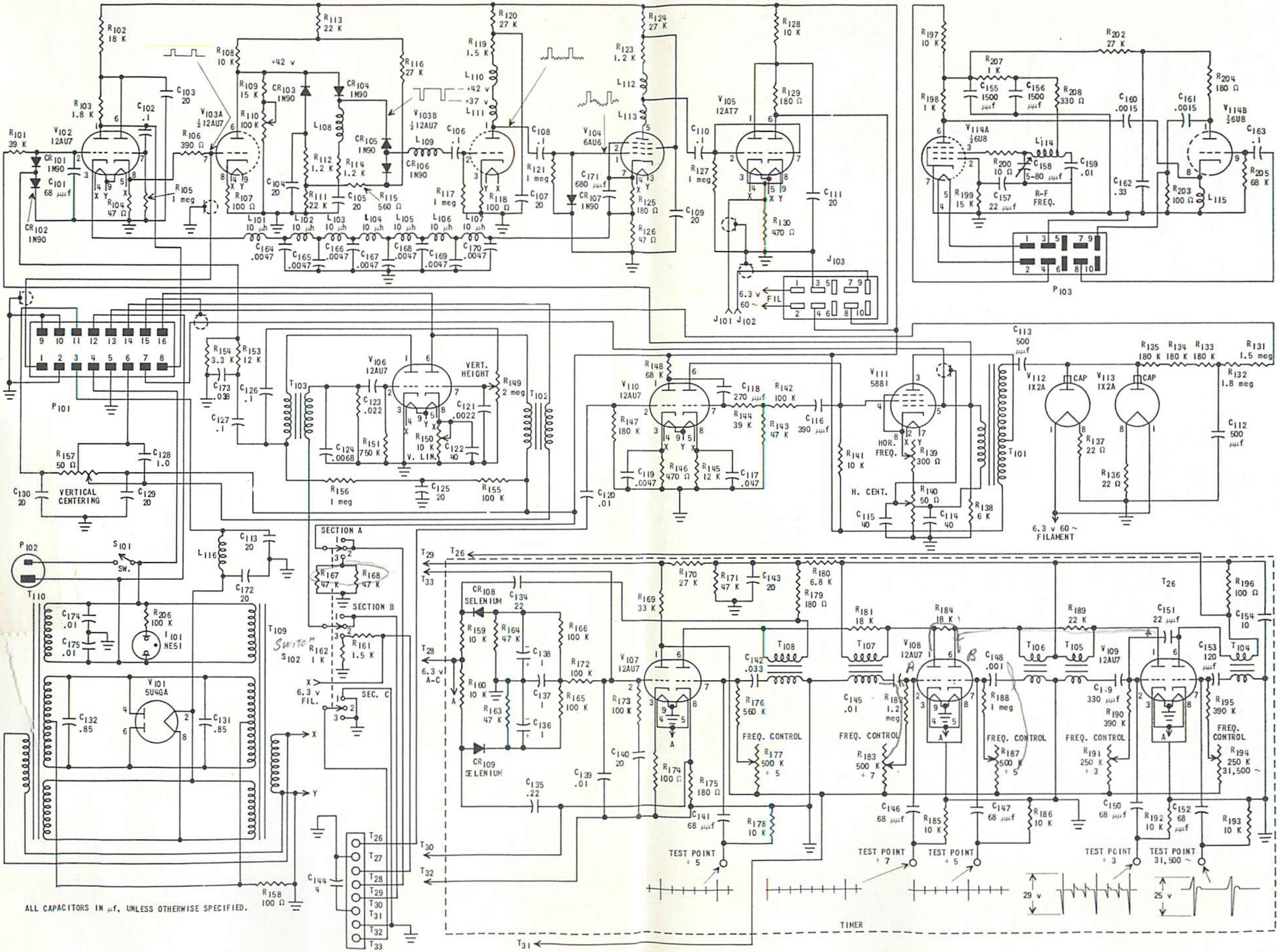

31,500 ~ MASTER OSCILLATOR V_{109B}
10,500 ~ OSCILLATOR ÷ 3 V_{109A}
2100 ~ OSCILLATOR ÷ 5 V_{108B}
300 ~ OSCILLATOR ÷ 7 V_{108A}
60 ~ OSCILLATOR ÷ 5 V_{107B}
AFC DISCRIMINATOR CR_{108}, CR_{109}
CONTROL AMPLIFIER V_{107A}
60 ~
PULSE AMPLIFIER V_{110}
HORIZONTAL OSCILLATOR AND AMPLIFIER V_{111}
BLANKING AND SYNC AMPLIFIER V_{102}
VERTICAL OSC. AND AMPLIFIER V_{106}
DELAY LINE
R-F TRANSMITTER V_{114}
R-F OUTPUT
VIDEO OUTPUT
HIGH VOLTAGE V_{112}, V_{113}
FIRST VIDEO AMPLIFIER V_{103A}
CHANNEL LIMITER CR_{103}, CR_{104}, CR_{105}, CR_{106}.
SECOND VIDEO AMPLIFIER V_{103B}
THIRD VIDEO AMPLIFIER V_{104}
VIDEO CATHODE FOLLOWER V_{105}
FROM CAMERA PRE-AMPLIFIER
TO VIDICON BLANKING AMPLIFIER

FIGURE 12



ALL CAPACITORS IN µf, UNLESS OTHERWISE SPECIFIED.

FIGURE 13

FROM OUR *Director's* NOTEBOOK

ACCENTUATE THE POSITIVE

When you apply for a job, a positive mental attitude can do more to achieve the results you want than any other approach. For one of the underlying laws of nature—of human behavior—is that things positive attract, influence, win over.

Remember you are offering a prospective employer something he wants. Otherwise he wouldn't consider you. He intends to use the know-how you have gained to help his company make a profit.

You have something to offer; the employer also has something to offer. Present a clear-cut, well organized explanation of your education and experience, emphasizing the things you do best which are needed on this particular job.

A positive attitude at this time toward your own qualifications—and how they **can** be of value to the employer—can help greatly in putting yourself across favorably and getting the job.

Yours for success,

W. C. DeVry

DIRECTOR

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